



## **TWO DAYS WORKSHOP ON FPGA BASED SYSEM DESIGN**

**(27<sup>th</sup> - 28<sup>th</sup> March, 2026)**

Organized by

**Department of Electronics and Communication Engineering**

**Indian Institute of Information Technology Design and Manufacturing, Kurnool – 518008, A.P.**

(An Institute of National Importance under Ministry of Education, Government of India)  
in association with

**C2S Project (Category III), Sponsored by MeitY, Government of India**

### **About the Institute**

Indian Institute of Information Technology Design and Manufacturing, Kurnool (IIITDMK) was announced in 2014 after receiving the assent of President of India to the Institutes of Information Technology Act, 2014, and its subsequent publication in the Gazette of India, Extraordinary, Part- II, Section I, on December 08, 2014. The institute was announced by Government of India to give effect to its obligation under the Andhra Pradesh reorganization act 2014. IIITDM Kurnool is fully funded by Ministry of Education. IIITDM Kurnool launched its academic program with the support of its mentor Institute, IIITDM Kancheepuram (Tamil Nadu), on August 2015 from the Kancheepuram campus. Consequent upon the approval of parliament, IIITDM Kurnool was accorded the status of Institute of National Importance by making an amendment in the IIIT act 2014 on August 03, 2017. In 2015, the Andhra Pradesh government allocated an area of 151 acres for the establishment of a permanent campus in Kurnool.

### **Who Can Attend the Workshop?**

This workshop is open to BTech/MTech/PhD students of Engineering/Technology/other allied Institutions in India.

### **Course Content**

|                           |   |
|---------------------------|---|
| Day-1 (Morning Session)   | Introduction to FPGA, Introduction to RTL Design, and Basics of Hardware-Software Codesign              |
| Day-1 (Afternoon Session) | Lab Practice on Custom IP Development and Hardware-Software Codesign using Xilinx Vivado with Zed Board |
| Day-2 (Morning Session)   | Custom IP Development using Matlab Simulink and Xilinx System Generator – Theory/Demo                   |
| Day-2 (Afternoon Session) | Lab Practice on Custom IP Development using Matlab Simulink and Xilinx System Generator with Zed Board  |

### **Other Details**

There is no registration fee for attending the workshop. Participants are responsible for their own travel and accommodation arrangements. No accommodation will be provided by the Institute. The participants can avail the services of canteen and mess at the Institute on pay & eat basis.

### **Registration**

Please fill the required details in the below registration link on or before 24 March 2026. Only limited seats (approx 40-45) are available. You are required to copy and paste this URL in the browser to fill the details.

[https://docs.google.com/forms/d/10sRXBk7dln7FazI58EOYRy3VSG4ONxtXNn\\_5nk5WmiY/edit](https://docs.google.com/forms/d/10sRXBk7dln7FazI58EOYRy3VSG4ONxtXNn_5nk5WmiY/edit)

### **Coordinators**

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