M. TECH.: VLSI Design & Microelectronics

Course Title	Course Code	Structure (I-P-C)		
Device Modelling	**EC 501**	**3**	**0**	**3**

Pre-requisite, if any: Electronic Devices and Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Model any kind of MOS Devices in 2-D or 3-D
CO2	Relate the models for further inclusion in circuits
CO3	Develop solution to overcome short channel issues
CO4	Develop various compact models appropriate for industry
CO5	Analyse the frequency response of MOS devices.

Syllabus:

Unit 1 :

Intuitive analysis of MOS Transistor- Two-Terminal MOS Structure – Flatband Voltage, Surface Condition, General Analysis, Inversion, Strong Inversion, Weak Inversion, SmallSignal Capacitance, Three-Terminal MOS Structure (7 hours)

Unit 2

Long-Channel MOS Transistor, Introduction All-Region Models, Strong Inversion Models, Weak Inversion Models, Source Reference vs. Body Reference, Effective Mobility (5 hours)

Unit 3

Small-Dimension Effects - Velocity Saturation, Channel Length Modulation, Charge Sharing, Drain-Induced Barrier Lowering, Hot Carrier Effects, Velocity Overshoot Ballistic Operation, Polysilicon Depletion (6 hours)

Unit 4

Small-Dimension Effects-Modelling for Circuits Simulation- Quantum-Mechanical Effects; Gate Current, Junction Leakage, Scaling and New Technologies, Approaches, and Properties of Good Models, Model Formulation Considerations, Parameter Extraction, Compact Models, Benchmark Tests (7 hours)

Unit 5

Small-Signal Modelling - Conductance Parameter Definitions and Equivalent Circuits, Conductance Parameters Due to Gate and Body Leakage, Transconductance, Source-Drain and Output Conductance, Capacitance Definitions and Equivalent Circuits, Capacitance Evaluation and Properties, y-Parameter Model, RF Models (11 hours)

Text Books

1. Y. Tsividis and C. McAndrew, “MOSFET modelling for Circuit Simulation”, Oxford University Press, 2011
2. C K Maiti, “Introducing Technology Computer-Aided Design (TCAD): Fundamentals, Simulations, and Applications”, Jenny Stanford Publishing; 1st Edition, 2017, ISBN: 978-9814745512.
3. Wu, Yung-Chun, Jhan, Yi-Ruei, “3D TCAD Simulation for CMOS Nanoeletronic Devices", Springer, 2017, ISBN 978-981-10-3066-6

References & Web Resources:

1. T. A. Fjeldly, T. Yetterdal, and M. Shur, “Introduction to Device Modeling and Circuit Simulation”, John Wiley, 1998.

2. Y. Taur and T. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, 1998.

3. Y. P. Tsividis, “Mixed Analog-digital VLSI Devices and Technology”, World Scientific Publishing Co Pte Ltd, 2002

4. C K Sarkar, “Technology Computer Aided Design: Simulation for VLSI MOSFET”, CRC Press, 1st Edition, 2013, ISBN: 978-1466512658. 5. J.-P. Colinge, “FinFETs and Other Multi-Gate Transistors”, Springer, 2008, ISBN: 978- 0- 387-71751-7

Course Title	Course Code	Structure (I-P-C)		
Analog IC Design	**EC 502**	**3**	**0**	**3**

Pre-requisite, if any: Analog Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the equivalent circuits of MOS based devices and analyze their performance.
CO2	Design analog VLSI circuits for a given specification.
CO3	Analyse the frequency response of the different configurations of an amplifier.
CO4	Appreciate the design features of the differential amplifiers.
C05	Apply principles of design to build one stage and two stage opamps.

Unit 1: CMOS Device Fundamentals Basic MOS Models, Device Capacitances, Parasitic Resistances, Substrate Models, Transconductance, Output Resistance, Frequency Dependence of Device Parameters Components and mismatch in CMOS process, models and Layout techniques Body effect, transit frequency. (6 hours)

Unit II Small signal analysis of MOSFET based amplifiers, Single Stage and Differential Amplifiers Common Source Amplifier, Source Degeneration, Source Follower, Common Gate Amplifier, Cascade Stage, Basic Differential Pair, Common Mode Response, Differential Pair with MOS Loads, Gilbert Cell, Device Mismatch Effects, Input Offset Voltage. cascade and cascode MOSFET based amplifiers (8 hours)

Unit III Noise in Resistor, capacitor, and MOSFET, spectral density Frequency Response of Amplifiers Miller Effect, CS Amplifier, Source Follower, CG Amplifier, Cascode Stage, Differential Amplifier, Multistage Amplifier. (6 hours)

Unit IV Current Mirrors, Current and Voltage Reference Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors, cascode current mirror, folded cascode multi stage, and Miller compensated op amps. Low Current Biasing, Supply Insensitive Biasing, Constant Transconductance Biasing, Temperature Insensitive Biasing, PTAT Current Formation, Impact of Device Mismatch. (7 hours)

Unit V Feedback, Stability and Frequency Compensation Feedback Topologies, Effect of Load, Modeling Input and Output Ports in Feedback Circuits, Multi Pole Systems, Phase Margin, Frequency Compensation, Voltage Controlled Oscillator (VCO), Phase Lock Loop (PLL). (6 hours)

Unit VI Operational Amplifiers Performance Parameters, One-Stage and Two-Stage Op-Amps, Gain Boosting, Comparison, Common Mode Feedback, Input Range, Slew Rate, Power Supply Rejection, Noise in Op-Amps, High Performance CMOS Op-Amp. arithmetic circuits, oscillators, active filters. (7 hours)

Text books

1. BehzadRazavi, “Design of Analog CMOS Integrated Circuits”, 2nd edition McGraw-Hill Education, 2016, ISBN: 978-0-07-252493-2
2. Baker, R. Jacob, “CMOS: Circuit design, Layout, and Simulation”, John Wiley & Sons, 2019.
3. P. R. Gray, P. J. Hurst, S. H. Lewis and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley and Sons, 5th Edition, 2009
4. P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2nd Edition, 2004

Course Title	Course Code	Structure (I-P-C)		
Digital IC Design	**EC 503**	**3**	**0**	**3**

Pre-requisite, if any: Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design digital systems using CMOS transistors.
CO2	Design the Layouts of various CMOS designs
CO3	Develop the sequential and Combinational Circuits with various CMOS topologies
CO4	Develop various Arithmetic & High performance circuits in full custom
C05	Design and analyse Memory Circuits

Syllabus:

Unit 1:

Introduction to MOS Device: First Glance at the MOS device MOS Transistor under static conditions, threshold voltage, channel length modulation, velocity saturation, hot carrier effect, sub threshold conduction, MOS structure capacitance.(5 hours)

Unit 2

MOS Transistor Device Modeling: Basic concepts-LEVEL1-LEVEL2-LEVEL3 modeling technique-various model comparison. Static CMOS inverter, performance of CMOS inverter, propagation delay sizing inverter for performance. (5 hours)

Unit 3

CMOS combinational logic design: Static CMOS designs, complementary CMOS design, power consumption in CMOS logic gates, design techniques to reduce switching activity, pass transistor logic, differential pass transistor logic, dynamic CMOS design, Domino CMOS logic, NPCMOS-logic style. (8 hours)

Unit 4

CMOS sequential logic design: multiplexer based latches, master slave edge triggered registers, non-ideal clock signals, low voltage static latches, static SR flip flop, Dynamic latches and registers, Dual edge registers, bi-stable sequential circuit Schmitt trigger-mono stable –Astable -sequential circuit - choosing a clocking strategy. (8 hours)

Unit 5

Timing metrics for combinational circuits, sequential circuits, Time budget issues, pipelining, folding/unfolding, resource sharing, metastability, synchronization, clock skew, setup/hold time of flip-flops, synchronization between multiple clock domains (6 hours)

Unit 6

CMOS subsystem design: Addition/Subtraction, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, memory elements, finite-State Machines. Memory Designs: SRAM, DRAM, ROM, PROM, EPROM, EEPROM, Flash, CAM (8 hours)

Text books

1. R. Jan, Chandrakasan, and A. Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson Education 2nd edition 2016.
2. N. H.E Weste and K. Eshraghian, Principles of CMOS VLSI Design, Addition Wesley, 2nd edition 1993.

3. 1. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, 3rd edition 2002.

Course Title	Course Code	Structure (I-P-C)		
Device modelling Practice	**EC504**	**0**	**3**	**2**

Pre-requisite, if any:

Course Outcomes: At the end of the course, the students will be able to:

CO1	Model any kind of MOS Devices in 2-D or 3-D
CO2	Relate the models for further inclusion in circuits
CO3	Develop solution to overcome short channel issues
CO4	Develop various compact models appropriate for industry
C05	Analyse the frequency response of MOS devices.

1. Introduction to Technology computer aided design (TCAD) tools; inputs and outputs of device and process simulations. (8 hours)
2. Device simulation: observing the terminal characteristics and distributions of carriers, current, field, potential and energy band diagrams within the device. (8 hours)
3. Process simulation: observation of device structure and doping profile Simulation of 2-D MOSFETs through device and process simulations (8 hours)
4. Simulation of novel 3-D transistors such as III-V HEMT, LEDs, FinFETs, GAA devices, solar cells etc, through device simulation (8 hours)
5. DC, AC, RF mixed mode and noise simulation for the devices (8 hours)

Course Title	Course Code	Structure (I-P-C)		
Analog IC Design Practice	**EC505**	**0**	**3**	**2**

Pre-requisite, if any: Analog Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyze the performance of various MOS amplifiers.
CO2	Design current mirrors for the various specifications.
CO3	Design and analyze differential amplifiers.
CO4	Design and analyze the performance of single stage OTA.
CO5	Apply principles of design to build one stage and two stage opamps.

1. Analysis of the nmos and pmos as active load and current source, MOS models implementation
2. Design of MOSFET based amplifiers (CS, CG, CD): Schematic and layout simulation using EDA tools.
3. Design of Cascode Amplifier.
4. Design of Current Mirrors.
5. Design of Differential Amplifiers.
6. Design of single stage OTA.
7. Design of single stage op-amp.
8. Design of 2-stage OPAMP and analysis of the properties Slew rate, CMRR,PSRR, etc.
9. Design of Op Amp based Circuits: Schematic and layout simulation using EDA tools.
10. Design of PLL.
11. Design of VCO.
12. Design of temperature insensitive biasing or PTAT.

Course Title	Course Code	Structure (I-P-C)		
Digital IC Design Practice	**EC506**	**0**	**3**	**2**

Pre-requisite, if any:

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design digital systems using CMOS transistors.
CO2	Design the Layouts of various CMOS designs
CO3	Develop the sequential and Combinational Circuits with various CMOS topologies
CO4	Develop various Arithmetic & High performance circuits in full custom
C05	Design and analyse Memory Circuits

1. DC characteristics of NMOS and PMOS and Parametric analysis
2. Scaling of other technology, calculator of non linearities lambda, body effect coefficient
3. DC characteristics of CMOS inverter
4. Transient characteristics of CMOS inverter
5. Basic gates using different Logic design style (PTL,TG,CMOS)
6. Universal gates using different Logic design style, Mux , encoders, decoders (PTL,TG,CMOS) with layout
7. Sequential Circuits Latch, Flipflop FSM etc
8. Building arithmetic circuits,
9. Design of memory SRAM
10. Timing analysis of Sept/Hold time analysing the issues

Course Title	Course Code	Structure (I-P-C)		
Mixed Signal Integrated Circuits	**EC507**	**3**	**0**	**3**

Pre-requisite, if any: Analog Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyze ADC and DAC using EDA tools
CO2	Apply the concepts for mixed signal MOS circuit
CO3	Analyze the signal to noise ratio and modeling of mixed signals
CO4	Understand the characteristics of ADC and DAC
C05	Design ADC and DAC using full custom ASIC

Syllabus:

1. Data converter fundamentals: Analog versus digital (or discrete time) signals, converting analog signals to data signals, sample and hold circuits, sample and hold characteristics, switched capacitor circuits, DAC specifications, ADC specifications.

2. Sample and hold and trans-linear circuits: Performance of sample-and-hold circuits – testing sample and holds, MOS sample-and-hold basics, examples of CMOS S/H Circuits, bipolar and BiCMOS Sample-and-Holds, Translinear gain Cell, trans-linear multiplier

3. DAC architectures: digital input code, R-2R ladder networks, current steering, charge scaling DACs, cyclic DAC, pipeline DAC.

4. ADC architectures: flash ADC, 2-step flash ADC, pipeline ADC, integrating ADC, successive approximation ADC.

5. Oversampling ADCs

Text Book(s):

1. Baker, R. Jacob, “CMOS: Mixed Signal Circuit Design”, John Wiley & Sons, 2019.

2. BehzadRazavi, “Principles of Data Conversion System Design”, Wiley

References & Web Resources:

1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, “Analog Integrated Circuit Design”, John Wiley & Sons

2. BehzadRazavi, “Design of Analog CMOS Integrated Circuits”, 2nd edition McGraw-Hill Education, 2016

Course Title	Course Code	Structure (I-P-C)		
VLSI PHYSICAL DESIGN & AUTOMATION	**EC508**	**3**	**0**	**3**

CO1	Able to place and partition the blocks while designing the layout for IC.
CO2	Able to solve the performance issues in circuit layout
CO3	Able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning,placement and routing
CO4	Able to analyze circuits using both analytical and CAD tools

Data Structures and Basic AlgorithmsBasic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms forPhysical design (8 hours)

Partitioning Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning Algorithms. Performance Driven Partitioning. (8 hours)

Floor Planning, Pin Assignment & TimingFloor planning, Chip planning, Pin Assignment Algorithms , Timing Concepts (8hours)

Global RoutingProblem Formulation, Classification of Global Routing, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path BasedAlgorithms, Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing.(8 hours)

Detailed RoutingProblem Formulation, Classification of Routing Algorithms, Single-Layer Routing Algorithms, Two-Layer Channel RoutingAlgorithms, Three-Layer Channel Routing Algorithms, Multi-Layer Channel Routing Algorithms, Switchbox RoutingAlgorithms (5 hours)

Over-the-Cell Routing and Via MinimizationOver-the-cell Routing, Via Minimization. Clock and Power Routing: Clock Routing, Power and Ground Routing. Compaction:Problem Formulation, Classification of Compaction Algorithms, One-Dimensional Compaction, Two-DimensionalCompaction. (6 hours)

Text books

1. N. Sherwani, Algorithms for VLSI Physical Design Automation, Springer Publications,1999.

2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, TMH, 1996

3. S. K. Lim, Practical Problems for VLSI Physical Design Automation, Springer Publications ,2008

Referencebooks

1. Hill & Peterson, Computer Aided Logical Design with Emphasis on VLSI , Wiley.1993.
2. W. Wolf, Modern VLSI Design: Systems on silicon, 4th edition, Pearson Education Asia ,1993

Course Title	Course Code	Structure (I-P-C)		
Digital Signal Processing and Architectures	**EC509**	**3**	**0**	**3**

Pre-requisite, if any: Digital Signal Processing, Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the concepts of digital signal processing: Filtering Techniques and Orthogonal Transformations.
CO2	Develop the hardware designs of various Digital Filtering.
CO3	Develop the hardware designs of various Orthogonal Transformations .
CO4	Design the co-processor for digital signal processing.
CO5	Analyse the multi rate signal processing.

Syllabus:

Unit-I: Digital filter design: Basics of folded/parallel design, FIR/IIR filter design, steepest- descent LMS algorithm, adaptive FIR filter design, multirate signal processing, polyphase decomposition, and filter banks. **(15 hours)**

Unit II – Discrete wavelet transform: Haar wavelet, 1D/2D/3D-Convolution based discrete wavelet transform architecture, 1D/2D/3D-(5,3) and (9,7) lifting based discrete wavelet transform architecture. **(10 hours)**

Unit III – FFT architectures: radix-2/4 SDF, MDC, parallel FFT architectures. **(5 hours)**

Unit IV – HEVC architectures: introduction to DCT, integer DCT architectures, and discrete Hadamard transform architectures. **(5 hours)**

Unit V – Motion Picture Estimation: Algorithms on motion picture estimation **(5 hours)**

Text Book(s):

1. S. K. Mitra, “Digital Signal Processing: A computer base approach”, Third edition, McGraw Hill Higher Education, 2006.
2. Y.T. Chan, “Wavelet Basics”, Kluwer Publishers, Boston, 1993.
3. Simon Haykin, “Adaptive filter theory”, Pearson Education, Fifth edition, 2014.

References & Web Resources:

1. V. Oppenheium and R. W. Schafer, “Discrete-time signal processing”, Second edition, Prentice Hall, 1999.

Course Title	Course Code	Structure (I-P-C)		
Mixed Signal Integrated Circuits Practice	**EC510**	**0**	**3**	**2**

Pre-requisite, if any: Analog Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyze ADC and DAC using EDA tools
CO2	Apply the concepts for mixed signal MOS circuit
CO3	Analyze the signal to noise ratio and modeling of mixed signals
CO4	Understand the characteristics of ADC and DAC
C05	Design ADC and DAC using full custom ASIC

Practice

1. Design and analysis of DACs in VLSI CAD tools (20 hours)
2. Design and analysis of ADCs in VLSI CAD tools (20 hours)

Syllabus

Course Title	Course Code	Structure (I-P-C)		
Digital Signal Processing and Architectures Practice	**EC512**	**0**	**3**	**2**

Pre-requisite, if any: Digital Signal Processing, Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the concepts of digital signal processing: Filtering Techniques and Orthogonal Transformations.
CO2	Develop the hardware designs of various Digital Filtering.
CO3	Develop the hardware designs of various Orthogonal Transformations .
CO4	Design the co-processor for digital signal processing.
CO5	Analyse the multi rate signal processing.

List of experiments:

1. Hardware/software co-design of signal processing operations (8 hours)
2. Digital Signal Co-processor design (8 hours)
3. Digital Filter Designs – FIR, IIR, Adaptive filters (8 hours)
4. Discrete Orthogonal Transform Designs – FFT, integer DCT, DHT, DWT (8 hours)
5. Experiments using DSP trainer kits (8 hours)

Text Book(s):

1. S. K. Mitra, “Digital Signal Processing: A computer base approach”, Third edition, McGraw Hill Higher Education, 2006.
2. Y.T. Chan, “Wavelet Basics”, Kluwer Publishers, Boston, 1993.
3. Simon Haykin, “Adaptive filter theory”, Pearson Education, Fifth edition, 2014.

References & Web Resources:

1. V. Oppenheium and R. W. Schafer, “Discrete-time signal processing”, Second edition, Prentice Hall, 1999.

Elective Courses

Course Title	Course Code	Structure (I-P-C)		
Analog and Mixed Signal Circuit Design	**EC566**	**3**	**0**	**3**

Pre-requisite, if any: Analog Electronics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyze complex analog integrated circuits using industry level analog IC Design tools
CO2	Design and analyze ADC and DAC using EDA tools
CO3	Design and analyze various MOSFET based arithmetic circuits.
CO4	Learn the various methods of power optimization in analog circuits.
CO5	Learn various circuits of design of Operational Amplifier

Syllabus:

Introduction: Review of single state MOS amplifiers, current mirrors, cascode current mirrors, active current mirrors, biasing techniques.

Op-amp design: Differential pair with current mirror load, single stage op-amp characteristics, single stage op-amp tradeoffs, telescopic cascode op-amp, folded cascode op-amp, two stage op-amp, fully differential single stage op-amp.

Data converter fundamentals: Analog versus digital (or discrete time) signals, converting analog signals to data signals, sample and hold circuits, sample and hold characteristics, switched capacitor circuits, DAC specifications, ADC specifications.

Data converters: DAC architectures – digital input code, R-2R ladder networks, current steering, charge scaling DACs, cyclic DAC, pipeline DAC, ADC architectures – flash ADC, 2-step flash ADC, pipeline ADC, integrating ADC, successive approximation ADC.

Phase locked loop: simple PLL, frequency/phase detectors, charge pump PLL, application as frequency multiplier.

Text Book(s):

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill International Edition 2016.
2. Baker, R. Jacob, CMOS: Circuit design, Layout, and Simulation. John Wiley & Sons, 2019.

References & Web Resources:

1. Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 2003.
2. Behzad Razavi, Fundamentals of Microelectronics, Second edition, Wiley, 2013
3. P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis And Design Of Analog Integrated Circuits, 5th edition, John Wiley & Sons, Inc., 2009.

Course Title	Course Code	Structure (I-P-C)		
Communication Protocols for Electronic System Design	**EC567**	**3**	**0**	**3**

Pre-requisite, if any: NIL

Course Aim: To teach fundamentals of communication protocols for designing electronic systems.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Quantitative analysis of individual components of industrial data communications.
CO2	Analysis and specification of serial communication protocol standards.
CO3	Understanding the error detection, cable shielding techniques to avoid stray pickups, noise.
CO4	Systematic understanding and development of industrial communication protocols.
CO5	Implement the different communication protocols for different applications

Syllabus:

Overview: Standards, OSI model, Protocols, Physical standards, Modern instrumentation and control systems, PLCs, Smart instrumentation systems, Communication principles and modes, error detection, Transmission, UART.

Serial communication standards: Standards, serial data communication interface standards, EIA-RS232 interface standard, RS-449, RS-422, RS-423 and RS-485 standards, Troubleshooting and testing with RS-485, GPIB standard, USB interface.

Error Detection, Cabling and Electrical Noise: Errors, Types of error detection, control and correction, copper and fiber cables, sources of electrical noise, shielding, cable ducting and earthling.

Modems and Multiplexers: Synchronous and Asynchronous modes, flow control, modulation techniques, types of a modem, modem standards, terminal and statistical multiplexers.

Communication Protocols: Flow control protocols, XON/XOFF, BSC, HDLC and File transfer protocols, OSI model and layers, ASCII protocols, Modbus protocol.

Industrial Protocols: Introduction to HART protocol, Smart instrumentation, HART physical layer, HART data link layer, HART application layer, ASD_i interface, Seriplex, CANbus, Device net, Profibus, FIP bus, Fieldbus.

Local Area Networks: Circuit and packet switching, Network topologies, Media access control mechanisms, LAN standards, Ethernet protocol, Token ring protocol.

References & Web Resources:

1. Practical data communications for instrumentation and control, John Park, Steve Mackay, Edwin Wright, Elsevier Newnes Publisher, 2008.

2. Computer Networks,Andrew Tanenbaum, Prentice Hall Professional Technical Reference, 2002.

Course Title	Course Code	Structure (I-P-C)		
RF and Microwave Integrated Circuits	**EC568**	**3**	**0**	**3**

Pre-requisite, if any: Electromagnetic Waves and Transmission Lines, and Analog Electronics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the differences in designing low frequency ICs, RFICs, and MMICs.
CO2	Analyse high frequency filters, couplers, amplifier, oscillators and mixer circuits.
CO3	Design high frequency filters, couplers, amplifiers.
CO4	Develop RFICs.
CO5	Develop MMICs.

Syllabus:

Electromagnetic Theory Review: Maxwell's Equations, Fields in Media and Boundary Conditions, The Wave Equation, General Plane Wave Solutions, Energy and Power, Transmission lines and waveguide solutions.

Transmission Line Theory: The Lumped-Element Circuit Model for a Transmission Line, Field Analysis of Transmission Lines, The Terminated Lossless Transmission Line, The Smith Chart, The Quarter-Wave Transformer, Generator and Load Mismatches, Lossy Transmission Lines, Transients on Transmission Lines.

Microwave Network Analysis: Impedance and Equivalent Voltages and Currents, Impedance and Admittance Matrices, The Scattering Matrix, The Transmission (ABCD) Matrix.

Impedance matching and tuning, Microwave filter design.

Noise and nonlinear distortion, active rf and microwave devices.

Microwave Power Amplifier, Low Noise Amplifier, Oscillator and Mixer Design.

Introduction to microwave systems.

Text Book(s):

1. David M Pozar, Microwave Engineering, 4th Edition, Wiley, 2013.
2. Behzad Razavi, RF Microelectronics, 2nd Edition, Pearson, 2011.

References & Web Resources:

1. Robert E Collin, Foundations for Microwave Engineering, 2nd Edition, Wiley, 2007.
2. I.D. Robertson , S. Lucyszyn, RFIC and MMIC Design and Technology: 13 (Materials, Circuits and Devices), Institution of Engineering and Technology, 2001.

Course Title	Course Code	Structure (I-P-C)		
Testing and Testability	**EC569**	**3**	**0**	**3**

Pre-requisite, if any: Digital Logic Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Identify the significance of testable design
CO2	Understand the concept of yield and identify the parameters influencing the same
CO3	Specify fabrication defects, errors and faults.
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage

Syllabus:

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models.

Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms. Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods.

Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method. D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design.

Classical scan based design, System level DFT approaches, Test pattern generation for BIST, and Circular BIST, BIST Architectures, and Testable memory design-Test algorithms-Test generation for Embedded RAMs.

Fault Diagnosis Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

Text Book(s):

1. M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990
2. Stroud, “A Designer’s Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002

References & Web Resources:

1. M. Bushnell and V. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2000
2. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House.
4. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers.
5. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
6. A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International.

Course Title	Course Code	Structure (I-P-C)		
VLSI Technology	**EC570**	**3**	**0**	**3**

Pre-requisite, if any: Electronic Devices

Course Outcomes: At the end of the course, the students will be able to:

CO1	Appreciate the intricacies involved in VLSI circuit fabrication.
CO2	Understand the various processes needed to fabricate the VLSI devices.
CO3	Learn fabrication steps for existing and coming generation devices.

Syllabus:

Theory

1. Introduction to VLSI Design, Bipolar Junction Transistor Fabrication, MOSFET Fabrication. (3 hours)

2. Crystal Structure of Si, Defects in Crystal, Crystal growth (3 hours)

3. Epitaxy, Vapour phase Epitaxy, Doping during Epitaxy, Molecular beam Epitaxy (3 hours)

4. Oxidation – Kinetics, Rate constants, Dopant Redistribution, Oxide Charges (5 hours)

5. Diffusion-Theory of Diffusion, Doping Profiles, Diffusion Systems Ion Implantation - Process, Annealing of Damages, Masking during Implantation (5 hours)

6. Lithography, immersion lithography, e-beam lithography (3 hours)

7. Etching-Wet Chemical Etching, Dry Etching, Plasma Etching, Si, SiO2, SiN and other materials (3 hours)

8. Deposition-Plasma Deposition, Metallization, Problems in Aluminium Metal contacts, Copper interconnects (3 hours)

9. IC BJT - LOCOS, Trench isolation, Poly-emitter-poly-base-BJT and its suitability for high-speed applications (4 hours)

10. MOSFET - Metal gate vs. Self-aligned Poly-gate, Tailoring of Device Parameters, CMOS Technology, Latch - up in CMOS, MOSFET structures with strained channels and high-k gate dielectrics, Bi-CMOS Technology, introduction to FINFETs (8 hours)

Text Book(s):

1. S. K. Ghandhi, “VLSI Fabrication Principles- Silicon and Gallium Arsenide”, Wiley Publications.

2. Y. Tsividis and C. McAndrew, “MOSFET modelling for Circuit Simulation”, Oxford University Press, 2011

References & Web Resources:

1. S. M. Sze, “VLSI Technology”, Tata McGraw Hill, 2008

2. J. Plummer, M. D. Deal, and P. B. Griffin, “Silicon VLSI Technology, Fundamentals, Practice and Modeling”, Pearson Higher Education, 2000

3. T. A. Fjeldly, T. Yetterdal, and M. Shur, “Introduction to Device Modeling and Circuit Simulation”, John Wiley, 1998.

4. Y. Taur and T. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, 1998.

Course Title	Course Code	Structure (I-P-C)		
Signal and Power Integrity	**EC571**	**3**	**0**	**3**

Pre-requisite, if any: Nil

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand the design guidelines to be followed in PCB design and IC packaging to prevent Signal and Power Integrity issues.
CO2	Analyze the physical structure and dimensions of the PCB elements and fit an appropriate circuit model.
CO3	Analyze the measured voltages and currents in the PCB and find the causes of the signal integrity issues.
CO4	Analyze the measured voltages and currents in the PCB and find the causes of the power integrity issues.
CO5	Design an optimal layout for a PCB to avoid signal and power integrity issues.

Syllabus:

Signal Integrity Is in Your Future: What Are Signal Integrity, Power Integrity, and Electromagnetic Compatibility?, Signal-Integrity Effects on One Net, Cross Talk, Rail-Collapse Noise, Electromagnetic Interference (EMI, Two Important Signal-Integrity Generalizations, Trends in Electronic Products, The Need for a New Design Methodology, A New Product Design Methodology.

Time and Frequency Domains: The Time Domain, Sine Waves in the Frequency Domain, Shorter Time to a Solution in the Frequency Domain, Sine-Wave Features, The Spectrum of a Repetitive Signal, The Spectrum of an Ideal Square Wave, Frequency Domain to the Time Domain, Effect of Bandwidth on Rise Time, Bandwidth and Rise Time, Bandwidth of Real Signals, Bandwidth and Clock Frequency, Bandwidth of a Measurement, Bandwidth of a Model, Bandwidth of an Interconnect.

Impedance and Electrical Models, The Physical Basis of Resistance, Capacitance, Inductance, and Transmissions lines.

Transmission Lines and Reflections, Lossy Lines, Rise-Time Degradation, and Material Properties, Cross Talk in Transmission Lines.

Differential Pairs and Differential Impedance, S-Parameters for Signal-Integrity Applications, The Power Distribution Network (PDN)

Text Book(s):

1. Bogatin, Eric. Signal and power integrity - simplified. Pearson Education, 2010.

References & Web Resources:

1. Johnson, Howard, Howard W. Johnson, and Martin Graham. High-speed signal propagation: advanced black magic. Prentice Hall Professional, 2003.
2. Johnson, Howard W., and Martin Graham. High-speed digital design: a handbook of black magic. Vol. 155. Englewood Cliffs, NJ: Prentice Hall, 1993.

Course Title	Course Code	Structure (I-P-C)		
Advanced Computer Architecture	**EC572**	**3**	**0**	**3**

Pre-requisite, if any: Digital Logic Circuits, Microprocessors and Microcontrollers

Course Outcomes: At the end of the course, the students will be able to:

CO1	Interpret the performance of a processor based on metrics such as execution time, cycles per instruction (CPI), Instruction count etc
CO2	Predict the challenges of realizing different kinds of parallelism (such as instruction, data, thread, core level) and leverage them for performance advancement
CO3	Apply the concept of memory hierarchy for efficient memory design and virtual memory to overcome the memory wall
CO4	Explore emerging computing trends, computing platforms, and design trade-offs Teaching Methodology
CO5	Design a data path of Harvard processor.

Syllabus:

1. Design Space Exploration and Optimizations: Performance metrics and performance enhancement techniques, basic concepts of parallel processing and pipelining, power dissipation in processors, power metrics, low-power design techniques, and Amdhal's law (5 hours)

2. Instruction set architecture design: Instruction set design, implementation and performance perspectives, relative advantages of RISC and CISC instruction set, processor datapath design using Von Nuemann and Harvard architectures. (5 hours)

3. Instruction-level parallelism (ILP): Pipeline data-path, data-dependence. challenges in ILP realization. instruction hazards and their solutions, out-of-order execution, control hazards, branch prediction, VLIW and superscalar processors, control hazards, static and dynamic prediction, dynamic instruction scheduling using score board, Thomosulo engine, and hardware speculation. (10 hours)

4. Memory systems: Brief overview of memory technologies (SRAM, DRAM, ROM, CAM, and flash), overview of memory hierarchy, cache design considerations, instruction vs. data caches, read, write, and replacement policies in cache, analysis of cache performance, and cache design for performance enhancement, cache coherence protocols, virtual memory organization. (10 hours)

5. Data Level Parallelism: Flynn's processor classification, SIMD, MIMD, GPU architectures (5 hours)

6. Multicore implementations: tightly and loosely coupled multicore architectures (5 hours)

Text Book(s):

1. J .L. Hennessy, D.A.Patterson, "Computer Architecture: a quantitative approach", Morgan Kaufmann, 5th edition, 2011, ISBN: 978-1558605961.
2. William Stallings, "Computer Organization and Architecture", Prentice Hall, 10th edition, 2015, ISBN-10: 013293633X, ISBN-13: 978-0132936330

References & Web Resources:

1. David E. Culler, Jaswinder Singh, and Morgan Kaufmann, “Parallel Computer Architecture: A Hardware/ Software Approach”, MK Publishers
2. C. Hamacher, Z. Vranesic and S. Zaky, “Computer Organization”, McGraw-Hill, 5th edition,2002, ISBN: 0072320869.
3. Andrew S. Tanenbaum, “Structured Computer Organization”, Prentice Hall, 6th edition, 2012, ISBN: 978-0132916523.
4. J.P. Shen and M.H. Lipasti, “Modern Processor Design", MCGraw Hill, Crowfordsville, 2005
5. John P. Hayes, “Computer Architecture and Organization”, McGraw Hill

Course Title	Course Code	Structure (I-P-C)		
FPGA-Based System Design	EC573	2	2	3

Pre-requisite, if any: Digital System design.

Course Outcomes: At the end of the course, the students will be able to:

CO1	Understand digital system design flow, HDL concepts, and RTL principles.
CO2	Apply arithmetic, logic, and FSM concepts in digital system design.
CO3	Analyse timing, synchronization, and pipelining issues in FPGA design.
CO4	Understand FPGA architecture and implementation flow.
CO5	Develop FPGA designs using hardware–software co-design, IP cores, and HLS.

Syllabus:

Unit 1:

Overview of digital system design methodologies, programmable logic devices, FPGA evolution, design abstraction levels, HDL-based design flow, RTL design principles. (6 hours)

Unit 2:

Combinational logic and sequential logic fundamentals, arithmetic and logic operations, design of Arithmetic Logic Unit (ALU), and finite state machine (FSM) modelling (Moore/Mealy). (6 hours)

Unit 3:

This unit introduces core timing and design concepts relevant to FPGA-based implementation. Topics include timing issues, pipelining, metastability, synchronization challenges, clock skew, and setup/hold time analysis of flip-flops. Synchronization between multiple clock domains using FIFO, PLL, and DLL is also covered. (6 hours)

Unit 4:

This unit covers FPGA internal architecture including configurable logic blocks, lookup tables, routing resources, memory elements, DSP components, and clocking structures. The FPGA implementation flow from synthesis to mapping, placement, and routing. (6 hours)

Unit 5:

This unit focuses on the hardware–software co-design methodology for FPGA platforms, including the development and integration of custom IP cores. (3 hours)

FPGA-Based System Design Practice

Pre-requisite, if any: Digital System Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Students will be able to design and simulate combinational and sequential circuits using HDL.
CO2	Students will implement FSM and FSMD architectures on FPGA hardware.
CO3	Students will analyze timing, resource utilization, and optimize FPGA-based designs.
CO4	Students will develop and test advanced digital systems such as FFT, filters, and floating-point units.
CO5	Students will gain hands-on experience with FPGA tools, debugging environments, and hardware validation.

1. Design and simulate basic combinational circuits (half adder, full adder, multiplexer, decoder) using HDL on FPGA
2. Implement sequential circuits such as flip-flops, shift registers, and counters using Verilog/VHDL.
3. Design a Mealy or Moore FSM and validate functionality using simulation and FPGA hardware.
4. Develop and implement an FSMD architecture combining data path and controller for a specific task.
5. Design and test a FIR digital filter using HDL, and analyze timing and resource utilization.
6. Implement a Radix-2 FFT architecture on FPGA and evaluate performance parameters.
7. Demonstrate hardware implementation, timing closure, and debugging.

Text Books

1. CMOS VLSI Design: A Circuits and Systems Perspective by Neil H. E. Weste & David Harris.
2. Pong P. Chu, FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version, John Wiley & Sons, 2008. ISBN: 978-0470185322.

References & Web Resources:

1. Wakerly, J. F., “Digital Design: Principles and Practices”, 4th Edition, Pearson, 2008

2. MironAbramovici, Melvin A Breuer, and Arthur D Friedman, “Digital Systems Testing and

Testable Designs”, Wiley-IEEE Press, 1994.

3. N. A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Bsp Books Pvt. Ltd.,

3rd edition, 2005.

4. Samir Palnitkar, “Verilog HDL - Guide to Digital design and synthesis”, Pearson Education,

3rd Edn, 2003.

Course Title	Course Code	Structure (I-P-C)		
VLSI Verification and Testing	**EC576**	**3**	**2**	**4**

Pre-requisite, if any: Digital Logic Circuits, VLSI Design

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyse complex VLSI systems using industry level Design and verification tools.
CO2	Understand the concept of yield and identify the parameters influencing the same
CO3	Specify fabrication defects, errors and faults.
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage

Syllabus:

Theory

1. Formal Hardware Verification: equivalence check and model check algorithms, compiler optimizations for formal verification, temporal logic, binary decision diagrams: OBDD, ROBDD, and BMD. (10 hours)
2. Introduction to VLSI Testing: Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. (3 hours)
3. Fault Modelling: Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms. Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods. (4 hours)
4. Automatic Test Pattern Generation: Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method. D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design. (8 hours)
5. DFT, scan chains, and BIST: Classical scan based design, System level DFT approaches, Test pattern generation for BIST, and Circular BIST, BIST Architectures, Boundary scan testing. (8 hours)
6. Memory and Delay Test: Testable memory design-Test algorithms-Test generation for Embedded RAMs, hazard free, robust, and non robust path delay fault tests, transition delay fault test. (8 hours)
7. Test Compression: Test Data Compression, Compression Methods and Decompression Methods. (4 hours)

Practice

1. Formal Verification: Basic UVM constructs & classes, design a basic test environment using UVM, System Verilog/HDL verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification. (20 hours)

2. VLSI Testing: Verify fault coverage of test patterns, simulate fault, apply test pattern, and observe output, Hands-on on Design for test (DFT) – insert test points, scan chains, to improve testability, Writing ATPG and Designs for Combinational and Sequential Circuits, Design of LFSR for BIST, Fault Models simulations and verifications, Structural Testing with Fault Models, and Implement path delay fault testing. (20 hours)

Text Books:

1. ZainalabedinNavabi, "Digital System Test and Testable Design using HDL Models and Architecture", 1st edition, Springer, 2010, ISBN: 978-1-4419-7547-8

2. Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSICircuits", Springer, 2004. ISBN: 7923- 7991-8.

3. SystemVerilog for Design: A Guide to Using System Verilog for Hardware Design and Modeling, 2 nd Edition, ISBN-13: 978-0387333991

4. Erik Seligman, Tom Schubert, andM V Achutha Kiran Kumar, "Formal Verification: An Essential Toolkit for Modern VLSI Design", MK Publishers.

References & Web Resources:

1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press.

2. Chris Spear, "SystemVerilog for Verification: A Guide to Learning the Testbench Language Features", Springer. 2012, ISBBN: 978-1461407140.

3. Donald Thomas, Logic Design and Verification Using SystemVerilog, 2016, ISBN: 1523364025.

4. UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology", 2013, ISBN: 0974164933.

Course Title	Course Code	Structure (I-P-C)		
RFIC Design	**EC578**	**3**	**0**	**3**

Pre-requisite, if any: Engineering Electromagnetics

Course Outcomes: At the end of the course, the students will be able to:

CO1	Analyze RF frequency filters, couplers, amplifier, oscillators and mixer circuits and LNA.
CO2	Design RF frequency filters, couplers, amplifiers, and LNA.
CO3	Design Oscillators, mixers and Phase Locked Loops
CO4	Develop RFICs.

Syllabus:

Introduction to RF and Wireless Technology: A Wireless World, RF Design Is Challenging, The Big Picture, Basic concepts in RF Design, General Considerations, Effects of Nonlinearity, Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation, Scattering Parameters, Analysis of Nonlinear Dynamic Systems, Volterra Series.

Communication Concepts: General Considerations, Analog Modulation, Digital Modulation, Spectral Regrowth, Mobile RF Communications, Multiple Access Techniques, Wireless Standards.

Transceiver Architectures: General Considerations, Receiver Architectures, Transmitter Architectures.

Low Noise Amplifiers and Mixer Design: General Considerations, Problem of Input Matching, LNA Topologies, Gain Switching, Band Switching, High-IP2 LNAs, Nonlinearity Calculations, General Considerations of Mixer, Passive Downconversion Mixers, Active Downconversion Mixers, Improved Mixer Topologies, Upconversion Mixers.

Passive Devices: General Considerations, Inductors, Transformers, Transmission Lines, Constant Capacitors.

Oscillators and Phase Locked Loop: Performance Parameters, Basic Principles, Cross-Coupled Oscillator, Three-Point Oscillators, Voltage-Controlled Oscillators, Tuning Range Limitations, LC VCOs with Wide Tuning Range, Phase Noise, Low-Noise VCOs, LO Interface, Mathematical Model of VCOs, Quadrature Oscillators, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase Noise in PLLs, Loop Bandwidth, Design Procedure.

Basics of Integer-N Frequency Synthesizers, Fractional-N Synthesizers and power Amplifiers, Transceiver Design Example.

Text Book(s):

1. BehzadRazavi, RF Microelectronics, 2nd Edition, Pearson, 2011.

References & Web Resources:

1. I.D. Robertson , S. Lucyszyn, RFIC and MMIC Design and Technology: 13 (Materials, Circuits and Devices), Institution of Engineering and Technology, 2001.

Course Title	Course Code	Structure (I-P-C)		
Mixed Signal Design	**EC579**	**3**	**2**	**4**

Pre-requisite, if any:

Course Outcomes: At the end of the course, the students will be able to:

CO1	Design and analyze various ADC and DAC using EDA tools
CO2	Apply the concepts for mixed signal MOS circuit
CO3	Analyze the signal to noise ratio and modeling of mixed signals
CO4	Design PLL circuits
C05	Design ADC and DAC using full custom ASIC

1. Analog and Discrete-Time Signal: Analog and discrete-time signal processing, introduction to sampling theory, Analog continuous-time filters: passive and active filters, Basics of analog discrete-time filters and Z-transform, Switched-capacitor filters. Non-linear & Dynamic Analog Circuits: Basic CMOS Comparator Design, Adaptive Biasing, Analog Multipliers. (5 Hours)
2. Data converter fundamentals: Analog versus digital (or discrete time) signals, converting analog signals to data signals, sample and hold circuits, sample and hold characteristics, switched capacitor circuits, DAC specifications, ADC specifications.(6 hours)
3. Sample and hold and trans-linear circuits: Performance of sample-and-hold circuits – testing sample and holds, MOS sample-and-hold basics, examples of CMOS S/H Circuits, bipolar and BiCMOS Sample-and-Holds, Translinear gain Cell, trans-linear multiplier (4 Hours)
4. DAC architectures: digital input code, R-2R ladder networks, current steering, charge scaling DACs, cyclic DAC, pipeline DAC.(7 hours)
5. ADC architectures: delta Sigma, flash ADC, 2-step flash ADC, pipeline ADC, integrating ADC, successive approximation ADC, Oversampling ADCs and layout issues (8 hours)
6. Phase Locked Loops: Voltage-mode signaling and data transmission, Current-mode signaling and data transmission, Introduction to frequency synthesizers and synchronization, Basics of PLL, AnalogPLL, Digital PLL, Delay locked loops (DLL) (6 hours)

Text Book(s):

1. Baker, R. Jacob, “CMOS: Mixed Signal Circuit Design”, John Wiley & Sons, 2019.

2. BehzadRazavi, “Principles of Data Conversion System Design”, Wiley References & Web

Resources:

1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, “Analog Integrated Circuit Design”, John Wiley & Sons

2. BehzadRazavi, “Design of Analog CMOS Integrated Circuits”, 2nd edition McGraw-Hill Education, 2016

3. Allen Halburg, “Analog Integrated Circuits”, Oxford

Course Title	Course Code	Structure (I-P-C)		
Compound Semiconductors Devices and Applications	**EC580**	**3**	**0**	**3**

Pre-requisite, if any: Electronics Devices and Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Interpret important parameters governing the high-speed performance of devices and circuits.
CO2	Model the properties of hetero junctions from the energy band diagram point of view.
CO3	Model the physics and operation and modeling of MESFETs.
CO4	Interpret the operation and performance parameters of HEMT, HBTs and Optoelectronics Devices.

Syllabus:

Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature - Materials properties: Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices - Band diagrams, homo and hetero junctions. (14 hours)

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor Field Effect Transistors (MESFETs): Basic features, Pinch off voltage and threshold voltage. (12 hours)

High Electron Mobility Transistors (HEMT): The generic Modulation Doped FET (MODFET) structure for high electron mobility realization, Principle of operation and the unique features of HEMT. Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high-speed applications. Optoelectronic Devices: Basic working principles and performance parameters of LED, Photodetectors and Solar Cell. (14 hours)

Text Book(s):

1. Sandip Tiwari, Compound Semiconductor Device Physics, Academic Press (1991), ISBN 0-12-691740-X.
2. S.M. Sze, High Speed Semiconductor Devices, Wiley (1990) ISBN 0-471-62307-5.
3. C.Y. Chang, F. Kai, GaAs High-Speed Devices: Physics, Technology and Circuit Applications, Wiley & Sons.
4. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons.
5. B. J. Baliga, Gallium Nitride and Silicon Carbide Power Devices, World Scientific, 2017.
6. David K. Ferry, Ed., Gallium Arsenide Technology, Howard W. Sams & Co., 1985
7. Avishay Katz, Indium Phosphide and Related materials: Processing, Technology and Devices, Artech House, 1992.
8. Ralph E. Williams, Modern GaAs Processing Methods, Artech (1990), ISBN 0-89006-343-5.

References & Web Resources:

1. M. S. Shur, M. S, *Physics of Semiconductor Devices*, Prentice-Hall, 1990.

2. Robert F. Pierret, Semiconductor Device Fundamentals, Addison-Wesley 1996.

3. https://nptel.ac.in/courses/117106089.

Course Title	Course Code	Structure (I-P-C)		
Organic Electronics	**EC581**	**3**	**0**	**3**

Pre-requisite, if any: Electronics Devices and Circuits

Course Outcomes: At the end of the course, the students will be able to:

CO1	Recognize the fundamentals of organic semiconductor devices.
CO2	Learn the charge generation and recombination mechanisms.
CO3	Infer about the organic light emitting diodes (OLEDs).
CO4	Learn about organic thin film deposition techniques and overview of various printing technologies.

Syllabus:

Introduction to organic semiconductor devices; Electronic Transitions, Excitons, and Energy transfer; Charge generation and recombination mechanisms; Polaron and Disorder models for charge transport; Space charge and Trap limited currents; Charge injection at metal/organic interface. (14 hours)

Organic light emitting diodes (OLEDs); Bilayer, Bulk-heterojunction, Inverted, and Tandem organic photovoltaic (OPV) devices; Carrier loss mechanisms in OPVs; Nanomorphology; Hybrid Perovskite solar cells and LEDs; Top and bottom contact organic thin film transistors (OTFTs). (12 hours)

Display driver circuits; Operating principles of organic lasers and memory devices; Device degradation mechanisms and Stability testing methods; Organic thin film deposition techniques and Overview of various printing technologies. (14 hours)

Text Book(s):

1. Suganuma Katsuaki, Introduction to Printed Electronics, Springer, 2014.
2. Stergios Logothetidis, Handbook of Flexible Organic Electronics - Materials, Manufacturing, and Applications, 1st Ed., Woodhead Publishing, 2014.
3. Eugenio Cantatore, Applications of Organic and Printed Electronics: A Technology Enabled Revolution, Springer, 2012.
4. Wolfgang Brütting and Chihaya Adachi, Physics of Organic Semiconductors, 2nd Ed., Wiley-VCH, 2012.
5. Anna Kohler and Heinz Bässler, Electronics Processes in Organic Semiconductors - An Introduction, 1st Ed., Wiley VCH, 2015.